DOCKET: FIS9-2003-0334 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR:	Jon A. Casey, et al.	EXAMINER:	Fernando L. Toledo
SERIAL NO.:	10/707,693	ART UNIT:	2823
FILING DATE:	January 5, 2004	DATE:	26 October 2005

FOR: A SUSPENSION FOR FILLING VIA HOLES IN SILICON AND METHOD FOR MAKING THE SAME

DECLARATION UNDER RULE 37 C.F.R. § 1.131

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

We, Jon A. Casey and Brian R. Sundlof, do hereby declare as follows:

1. We are employees of International Business Machines Corporation ("IBM"), the assignee of the above-identified patent application entitled "A SUSPENSION FOR FILLING VIA HOLES IN SILICON AND METHOD FOR MAKING THE SAME." We are co-inventors of the invention described and claimed in the above-identified application.

2. This is a declaration under the provisions of 37 C.F.R. § 1.131 for the purpose of swearing back of a reference that was cited in the subject application. This declaration establishes facts showing conception and reduction to practice of this invention in this country prior to the December 5, 2003 filing date of Edelstein, et al. (U.S. Patent

Application Publication No. 2005/0121768 A1) cited against this application, and due diligence from a time prior to that date until the application was filed.

3. The claimed invention in the above-identified application was conceived by us in the United States prior to December 5, 2003. This is evidenced by the copy of a portion of an invention disclosure form created by inventor Jon A. Casey, Ph.D., describing the invention disclosed in the subject patent application. Exhibit A. The Exhibit A disclosure describes the use of a method for metallizing either blind or through vias in silicon. It teaches forming a low coefficient of thermal expansion composite or suspension, relative to pure metals such as copper, and filling the via holes in the silicon with the newly developed paste. It discloses the controlled sintering of copper and a CTE matched material. The disclosure further teaches having the paste contain a high solids loading in suspension. The sintering temperature is taught to be high enough to allow the metal particles in the paste to sinter together, and low enough so that the CTE particles remain unsintered.

4. The disclosure of Exhibit A was created, and is dated, prior to December 5, 2003, the filing date of the Edelstein, et al., patent. Actual dates and the material not pertinent to conception and reduction to practice of the invention have been redacted in view of their confidential nature.

5. The following chart compares the steps of the claimed method in detail with the teachings in the original disclosure and Exhibit A:

CLAIM 1	**ORIGINAL DISCLOSURE**
A method of filling vias in a silicon substrate, said method comprising:	"a new metallization process and material system has been developed for metalizing either blind or through vias is silicon." Detailed Embodiment, Ex. A.

obtaining a silicon substrate having a plurality of via holes;	"Provide a means to fill 200 micron deep, 15-50 um diameter, blind vias and lines in Silicon wafers with a conductive material." Ex. A, p.2.
filling said vias with a high-solids loading paste including a conductor material and a low CTE additive material; and	"The concept involves forming a low CTE (relative to pure metals such as Cu, Ag or Au) composite paste, and filling the vias in the silicon with said paste." Detailed Embodiment, Ex. A.
sintering said silicon substrate and paste at a temperature for densification of said metal but not said low CTE additive material.	"Controlled sintering of Cu and CTE Matched insulator – Achieve full densification of Cu to maximize electrical performance – Partial densification of dielectric phase to minimize overall composite shrinkage and insure complete via fill post sinter." Ex. A, p.2. "[T]he sintering temperature is selected such that the metal particles will sinter together completely, while the low CTE particles remain unsintered." Detailed Embodiment, Ex. A.

6. The disclosure form and Detailed Embodiment of Exhibit A was submitted to IBM's patent attorneys prior to December 5, 2003.

7. We also reduced to practice the invention described in the disclosure and Detailed Embodiment of Exhibit A in the United States prior to December 5, 2003. This reduction to practice was a "working implementation" of laboratory samples as noted on page 2 of Exhibit A. The reduction to practice implemented all of the steps and limitations described in claim 1 of the subject patent application.

8. In addition to the reduction to practice, we worked diligently with patent counsel from a time before the date of the Edelstein reference, December 5, 2003, until the January 5, 2004 filing date of the subject application.

9. We received notice from Ira Blecker, the IBM patent attorney responsible for the subject patent application, that the patent application for the invention described in the Disclosure (assigned IBM Docket No. FIS9-2003-0334) would be prepared by outside counsel, in the law firm of DeLio & Peterson LLC, New Haven, Connecticut.

10. Between August 2003 and December 2003, we had correspondence and at least one telephone conference with Attorney Robert Curcio of DeLio & Peterson, LLC regarding the instant invention.

11. In November 2003, we received from Attorney Curcio a draft application of the instant invention including a specification, a set of drawings, and a set of claims.

12. We are informed that on December 3, 2003, Attorney Curcio sent the completed patent application on the instant invention to Attorney Blecker for execution by us and filing with the U.S. Patent and Trademark Office ("PTO").

13. On December 16, 2003, we executed the declaration for the instant application.

14. We declare further that all statements made herein on information and belief are believed to be true; and further that these statements and the like so made are punishable by fine or imprisonment or both, under § 1001 of Title XVIII of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issuing thereon.

Jon A. Casey — Date: 10/25/05

Brian R. Sundlof — Date: 10/25/05

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date indicated below as first class mail in an envelope addressed to Mail Stop _____, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Name: Barbara E. Browne Date: October , 2005 Signature:

ibmf100411000_r131_decl.doc

Disclosure FIS8-2002-0292

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By: Jon Casey **Created On:** [redacted]
Last Modified By: Jon Casey **Last Modified On:** [redacted]

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

***Title of disclosure (in English)**

Blind Via Filling in Si Wafers: Materials and Methods

Summary

Status	Under Evaluation
Final Deadline	
Final Deadline Reason	
Processing Location	FIS
Functional Area	(DF3) DF3 ... SCHNEIDER/ Knickerbocker: Product Dev.
Attorney/ Patent Professional	Ira Blecker/Fishkill/IBM
IDT Team	Mukta Farooq/Fishkill/IBM; John Knickerbocker/Fishkill/IBM; Peter Berasi/Poughkeepsie/IBM; Robert Haas/Fishkill/IBM; Mark Takacs/Fishkill/IBM; Wai Ma/Poughkeepsie/IBM; Joseph Sullivan Jr/Fishkill/IBM
Submitted Date	[redacted]
*Owning Division	MD
Incentive Program	
Lab	
Technology Code	150P
PVT Score	To calculate a PVT score, click on "Patent Value Tool" in the action bar.

Inventors with a Blue Pages entry

Inventors: Jon Casey/Fishkill/IBM, Brian R Sundlof/Fishkill/IBM

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Sundlof, Brian R.	[redacted]	29/08JA	532-1736	Humenik, James N.

> denotes primary contact

Inventors without a Blue Pages entry

IDT Selection

Attorney/Patent Professional: Ira Blecker/Fishkill/IBM

IDT Team: Mukta Farooq/Fishkill/IBM, John Knickerbocker/Fishkill/IBM, Peter Berasi/Poughkeepsie/IBM, Robert Haas/Fishkill/IBM, Mark Takacs/Fishkill/IBM, Wai Ma/Poughkeepsie/IBM, Joseph Sullivan Jr/Fishkill/IBM

Response Due to IP&L: [redacted]

***Main Idea**

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

OBJECTIVE
Provide a means to fill 200 micron deep, 15-50 um diameter,
blind vias and lines in Silicon wafers with a conductive material.
R<0.03
C(to Si)<0.5pF
3 on 6 C4 pitch
(i.e., 50 um x 200 um deep vias with conductivity >1/10x Cu)

TECHNICAL REQUIREMENTS
1.) High Solid's Loading Suspension of Cu and Insulator
- Maximize Solid's In Via To Reduce Overall Sintering Shrinkage
2.) Percolation Controlled Composite Structure of Cu and Insulator
- Establish Minimum Cu Percentage for Electrical Requirements
3.) Controlled Sintering of Cu and CTE Matched Insulator
- Achieve Full Densification of Cu to Maximize Electrical Performance
- Partial Densification of Dielectric Phase to Minimize Overall Composite Shrinkage and Insure Complete Via Fill Post Sinter
- Final Structure Will Be an Interpenetrating Dense Copper Network Through a Porous Network of Matched CTE Glass
4.) Manufacturable Process for Filling of Blind Via Hole
- Need to Develop Process With Complete Fill and Minimum Drying Shrinkage
- Suspension Solid's Loading Approaching Particle Packing Limits

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?
New slurry technology provides a new material system that provides excellent fill behavior as well as excellent electrical and microstructural characteristics

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?
Yes. Electrolytic plating of the features as well as traditional paste filling have been attempted. However, the new material sytems provides superior processing as well as superior electrical properties.

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.
At present, the new material system has been utilized in lab samples only. Full scale prototype builds will be initiated [redacted] This new technology is critical to the sucess of the System on a Package technology being developed at IBM Research

***Critical Questions (Questions 1-9 must be answered in English)**

***Question 1**
On what date was the invention workable? [redacted] **Please format the date as MM/DD/YYYY**
(Workable means i.e. when you know that your design will solve the problem)

***Question 2** Is there any planned or actual publication or disclosure of your invention to anyone outside IBM?	○ Yes ● No
If yes, Enter the name of each publication or patent and the date published below. Publication/Patent: Date Published or Issued:	
Are you aware of any publications, products or patents that relate to this invention?	○ Yes ● No
If yes, Enter the name of each publication or patent and the date published below. Publication/Patent: Date Published or Issued:	

***Question 3** Has the subject matter of the invention or a product incorporating the invention been sold, used internally in manufacturing, announced for sale, or included in a proposal?	○ Yes ● No
Is a sale, use in manufacturing, product announcement, or proposal planned?	○ Yes ● No
If Yes, identify the product if known and indicate the date or planned date of sale, announcements, or proposal and to whom the sale, announcement or proposal has been or will be made. Product: Version/Release: Code Name: Date: To Whom: If more than one, use cut and paste and append as necessary in the field provided.	

***Question 4** Was the subject matter of your invention or a product incorporating your invention used in public, e.g., outside IBM or in the presence of non-IBMers?	○ Yes ● No
If yes, give a date. **Please format the date as MM/DD/YYYY**	

***Question 5** Have you ever discussed your invention with others not employed at IBM?	○ Yes ● No
If yes, identify individuals and date discussed. Fill in the text area with the following information, the names of the individuals, the employer, date discussed, under CDA, and CDA #.	

***Question 6** Was the invention, in any way, started or developed under a government contract or project?	○ Yes ● No ○ Not sure
If Yes, enter the contract number	

***Question 7** Was the invention made in the course of any alliance, joint development or other contract activities? If **Yes**, enter the following:	○ Yes ● No ○ Not Sure
Name of Alliance, Contractor or Joint Developer	

Contract ID number
Relationship contact name
Relationship contact E-mail
Relationship contact phone

***Question 8**
Have you, or any of the other inventors, submitted this same invention disclosure or similar invention disclosure previously?

○ Yes
● No

If Yes, please provide disclosure number below:

***Question 9**
Are you, or any of the other inventors, aware of any related inventions disclosures submitted by anyone in IBM previously?

○ Yes
● No

If Yes, please provide the docket or disclosure number or any other identifying information below:

Question 10
What type of companies do you expect to compete with inventions of this type? *Check all that apply.*

- ☒ Manufacturers of enterprise servers
- ☒ Manufacturers of entry servers
- ☒ Manufacturers of workstations
- ☒ Manufacturers of PC's
- ☒ Non-computer manufacturers
- ☐ Developers of operating systems
- ☐ Developers of networking software
- ☐ Developers of application software
- ☐ Integrated solution providers
- ☐ Service providers
- ☐ Other (Please specify below)

Question 11
If the invention relates to a product or service that is outside the scope of your business unit, please recommend IBM business unit(s), IBM location(s) or individual(s) within IBM that you think would provide a good evaluation of your invention:

Patent Value Tool (Optional - this may be used by the inventor and attorney to assist with the evalua
(The Patent Value tool can be used by the inventor(s) to determine the potential licensing value of your invention.)

Market

What is the anticipated annual market size (in dollars) that will be captured by your invention?

CLAIMS

Question 1 - How new is the technical field?

Question 2 - How central is the invention to the product(s) which might be expected to contain the

invention?

Question 3 - What is the scope of the claim?

PORTFOLIO NEED

What are the portfolio needs in the area of your invention?

EXPLOITATION & ENFORCEMENT

Question 1 - How easily can the use of the invention by a competitor be detected?

Question 2 - How easily can the use of the invention be avoided by a competitor?

BUSINESS VALUE

Question 1 - What percentage of the companies producing products in the field of this invention might use this invention?

Question 2 - What is the value of this patent to current or anticipated Alliance Activity between IBM and other companies?

Question 3 - What is the value of this patent to current or anticipated Technology Transfer Activity between IBM and other companies?

Question 4 - Does it result in prestige to IBM?

Post Disclosure Text & Drawings

Enter any additional information relating to this disclosure below:

(Form Revised 12/17/97)

DETAILED EMBODIMENT

Background

Packaging of integrated circuits (IC's or chips) is required for electrical interconnection, thermal management, as well as mechanical integrity of the IC. Numerous types of electronic packages are available. Two common forms of high-end packages are multilayer ceramic (MLC) substrates and multilayer organic substrates. These two packaging technologies are used for most high end applications with each having particular advantages and disadvantages. The key advantages for ceramic packages include, 1) close thermal expansion matching of the substrate to that of the IC, 2) good thermal conduction to aid in heat dissipation from the IC, and 3) a high level of integration to allow for complex wiring schemes. Some common limitations of ceramic packages are associated with the inferior dielectric properties (higher k values) of the ceramic, relative to organic packaging materials, as well as larger feature sizes in the structure, due to limitations associated with thick film processing.

Organic packaging technology improves on some of the limitation associated with ceramic packaging technology. Organic packages are mainly produced using photo-patterning processes which are capable of producing much smaller wiring features compared to their ceramic counterparts. This allows for increased circuit densities and allowing for more compact designs. However, organic packages typically have lower thermal conductivity and a much higher coefficient of thermal expansion (CTE), when compared to ceramic substrates. These limitations can result in problems associated with thermally induced stresses during processing and use of organic packages and can lead to inferior reliability for the assembled module (IC + substrate).

The thermal stresses are becoming increasingly important for the new chip structures being manufactured with low k and ultra low k dielectric materials, which have inferior mechanical properties relative to the historical oxide dielectrics used in previous generations of chips. In addition, the packaging technology will require improved circuit densities, as well as, improved thermal management.

Silicon would be an ideal candidate for complex electronic packaging. Since most chips are made with silicon, the thermal expansion of the chip would be essentially identical to that of the substrate, virtually eliminating thermally induced stresses between the chip and the substrate. Additionally, processes are well established to produce high density, copper based, single or multilevel circuitry on silicon.

IC packages contain numerous wiring levels with circuits varying in scale from very fine to fairly large. The larger scale wiring levels are required for power distribution, as well as electrical interconnections from the chip package to the next level (second level) of interconnection, typically a circuit board or card. Feature sizes approach 100 to 1000 microns for second level interconnection. A processing issue associated with these large feature sizes in silicon is related to the formation of z axis interconnections (vias) in the silicon. Formation of vias in silicon is typically performed using photo-patterning, followed by some form of chemical etching (typically reactive ion etching). These processes can readily form large diameter vias, either blind or though vias. Metallization of the vias is typically performed using some form of vapor deposition

(CVD or PVD) and/or electrochemical plating. A major issue with these metallization schemes, especially for large diameter vias, is that the deposited via metallurgy induces very high stresses in the silicon in the immediate area surrounding the vias. These stresses are the result of the thermal expansion mismatch between the silicon and the via metallurgy. Since the magnitude of the crack driving force (K) scales with the via diameter, as the via diameter increases, the thermal stresses associated with the metallized vias can result in cracking of the silicon adjacent to the vias. These cracks can result in electrical and/or mechanical failure of the silicon package.

Ideally one would like to develop a method to fill either blind or through vias in silicon with a conductive material which has a coefficient of thermal expansion (CTE) closer to that of silicon. Additionally, one would like the said conductive material to have excellent conductivity. Lastly, one would like to completely fill the via with said conductive material since large gaps and/or voids at the conductor/silicon interface may degrade the mechanical integrity of the device.

Invention

To achieve the said fore mentioned ideal package attributes, a new metallization process and material system has been developed for metallizing either blind or through vias in silicon. The concept involves forming a low CTE (relative to pure metals such as Cu, Ag or Au) composite conductive paste, and filling the via holes in the silicon with said paste. The conductive paste is a composite which contains a metal powder, or a mixture of metal powders such as Cu, Au, or Ag, as the conductive phase(s), and a low CTE additive(s) to reduce the overall CTE of the paste. The low CTE additives can be a conductor, insulator or a mixture of both. However, most conductive materials have relatively high CTE's compared to low CTE insulators. As such, to achieve a significant reduction in the composite CTE, a mixture of a good conductor, such as copper, with a low CTE insulating phase, can result in a composite material with good electrical properties, as well as significantly lower CTE's, relative to the pure metal.

To achieve good electrical performance, as well as a low CTE, the paste system must be optimized in terms of amount of conductive phase, relative to amount of low CTE phase. We have found that an amount of conductor particles from 20 -80 volume percent, to be an effective range, with a preferred range being 25 to 50 volume percent and a more preferred range being 30 to 45 volume percent. For the low CTE phase, we have found that a magnesium aluminosilicate glass, when added to the paste in a range of 20 to 80 volume percent to be an effective additive, with a preferred range of 50 to 75 volume percent and a more preferred range of 55 to 70 volume percent. The above volume percent calculations are based on solid's content only (i.e., conductor and low CTE particles only) and do not include the other paste components such as solvent or dispersants. Other effective low CTE additives we have tried, but are not limited too, include, silica, corderite, spodumene, borosilicate glasses, mullite, beta eucryptite, tungsten or molybdenum.

To achieve a completely filled via, the paste system must contain a very high solid's loading. As the solid's loading of a suspension increases, the amount of drying shrinkage that occurs during solvent removal is greatly reduced. When a solid's loading above 50 volume percent is achieved in a suspension, the amount of drying shrinkage is typically very low. As such, a high solid's

loading, as well as a fairly low suspension viscosity, is required to achieve good via fill for the above particulate suspensions: To meet these requirements, both aqueous and non-aqueous based suspensions were employed. Suspension solid's loadings above 50 volume percent were achieved with suspension viscosity's below 1000 centipoise. A typical suspension is listed below:

Ingredient	Suspension Volume Percent	Sintered Volume Percent
Copper	17.2	32.8
Magnesium aluminosilcate glass	35.2	67.2
Dispersant	1.5	0
Water (solvent)	46.1	0

The above paste can be used to fill either through vias or blind vias using a simple vacuum filling process. A silicon package can be placed in a vacuum chamber, and a vacuum is drawn using a conventional mechanical vacuum pump. While under vacuum, the above suspension can be used to flood the surface of the silicon package, which contains empty vias. The suspension will fill the vias through capillary action. The pressure can then be slowly raised to ambient pressure, during which time, additional suspension is pushed into the via structure. Excess material can be simply wiped off the surface, and the filled vias can be dried by conventional means.

After drying, the via is filled with a mixture of conductive metal particles, and for the above example, low CTE glass particles. Without additional processing, the material is essentially an insulator. In order to form a good conductor, the filled via needs to be sintered, in order to allow the metal conductive particles to fuse together and form a continuos network of metal. However, in order to avoid bulk shrinkage of the filled via, the sintering temperature is selected such that the metal particles will sinter together completely, while the low CTE particles remain unsintered. Since the majority of the via is filled with low CTE material, during sintering, the metal conductor undergoes densification, but the low CTE phase retains it's original structure and dimension. As such, the mixture undergoes a minimal (less than 5%) bulk volumetric shrinkage. This insures that no large gaps or cracks are formed within the via or at the via to silicon interface during sintering. This sintering behavior is obtained by careful selection of the type, amount and particle size of the metal conductors, as well as the low CTE phase. Ideally one would like the metal conductor to sinter well below the onset of the densification of the low CTE phase. We have found that a 100°C delta in sintering temperature onset between the metal conductor and the low CTE phase, to be a sufficient processing window to allow for a continuos network of metal conductor to form within the porous network of low CTE material. The metal network has excellent electrical conductivity, roughly an order of magnitude lower than fully dense pure conductor but still sufficient to provide the necessary resistivity of the system.